IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF WISCONSIN

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SANDISK CORPORATION,

ORDER

Plaintiff,

v.

10-cv-243-bbc

KINGSTON TECHNOLOGY CO., INC., KINGSTON TECHNOLOGY CORP., IMATION CORP., IMATION ENTERPRISES, CORP., MEMOREX PRODUCTS, INC.,

Defendants.

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In this case for patent infringement, the parties have filed cross motions for the construction of several terms in U.S. Patents Nos. 7,397,713; 7,492,660; 7,657,702; 7,532,511; 7,646,666; and 7,646,667, all of which are related to flash memory technology.[1] I will hold a hearing on the parties' disputes about all but one of the claim terms for which they seek construction, "registers."

In the magistrate judge's preliminary pretrial conference order, dkt. #69, at 2, he explained that it would be each "party's burden to persuade the court that construction of each specified term is necessary to resolve a disputed issue concerning infringement or

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[1] All six patents are divisionals or continuations of patents asserted in separate action pending before this court, Cases Nos. 07-cv-605 and 07-cv-607, and share the same specifications with the patents in those cases.

invalidity." The purpose of that requirement is to avoid deciding abstract questions that have no bearing on the lawsuit. Federal courts "possess no . . . authority to issue advisory opinions." Citizens for a Better Environment v. Steel Co., 230 F.3d 923, 927 (7th Cir. 2000). For 15 of the 16 requested claim terms, the parties explained how their disputes about the meaning of the term are related to disputes about whether the accused products are infringing or the patents invalidated by prior art. (The parties seek construction of more than 16 separate phrases, but there are only 16 discrete disputes related to the meaning of those phrases. I refer to the groups of phrases related to each single dispute as a "claim term" for the sake of simplicity.) Neither party explains why the term "registers" should be construed.. Plaintiff simply states that the parties agree that the term should be construed. Even if this is true (defendant seems to disagree, asserting that no construction of the term is necessary), this is beside the point. Regardless whether the parties agree to present a claims construction dispute to the court, it should not be resolved unless it is tied to an infringement or invalidity dispute.

Accordingly, I conclude that the parties have failed to meet their burden to show that the term "registers" requires construction. If either party later determines that construction of "register" is necessary, it will have to raise that issue at summary judgment or trial. As for the remaining 15 terms, because the parties have met their burden with respect to these terms, and because it would be beneficial to hear oral argument on matter, a claims

construction hearing will be held on January 14, 2011 at 9:00 a.m, the date designated in the preliminary pretrial conference order.

ORDER

IT IS ORDERED that a hearing will be held on January 14, 2011 at 9:00 a.m regarding the parties' disputes on the meaning of the following claim terms:

1. From United States Patents Nos.7,397,713 and 7,492,660:

   A. "wherein said controller includes an address register file, and is such as to allow a host logical address from said host system to be converted to a physical address of said nonvolatile semiconductor flash memory based on data stored in said address register file," ('713 pat., cl. 1) and "wherein said controller includes a register file to store defect mapping data" ('713 pat., cl. 11); and

   B. "receiving a logical address at a controller for the flash memory array and determining that the logical address corresponds to a defective memory location," ('660 pat., cl. 1) and "a selecting unit receiving a logical address for the flash memory array, determining that the logical address corresponds to a defective location ('660 pat., cl. 15)

2. From United States Patent No. 7,657,702:

   A. "logical address(es)," ('702 pat., passim), "programming a first group of a plurality of pages in at least the first and second blocks with original data, the pages of original data having logical addresses associated therewith," ('702 pat., cl. 1), "programming original data into individual ones of a first plurality of pages in at least a first block, the original data having logical addresses associated therewith," ('702 pat., cl. 16), "programming the received plurality of pages of original user data into a first plurality of pages of storage elements," ('702 pat., cl. 24) and "programming the received plurality of pages of original data into a first plurality of pages of storage elements" ('702 pat. cl. 33);

B. page ('702 pat., passim);

C. sub-array ('702 pat., cls. 1, 33; also in'511 pat., cl. 1 and '667 pat., cl. 1);

D. "an updatable data structure that links one or more physical addresses of the first group of pages with one or more of the logical addresses associated with the data stored therein," ('702 pat., cl. 1) and "updatable address information that links physical addresses of the first and second blocks storing original and updated data with the logical addresses associated with the stored data" ('702 pat., cl. 16);

E. "the memory controller being characterized by performing at least the following operations: (a) responds to receipt . . . by programming the received plurality of pages of original user data into a first plurality of pages of storage elements in the preset order in at least a first one of the blocks," ('702 pat., cl. 24) and "a memory controller connected with the interface and with the plurality of blocks of storage elements, the memory controller being characterized by performing at least the following operations: . . . (b) responds to receipt . . . by programming the received plurality of pages of original data into a first plurality of pages of storage elements in a first plurality of blocks forming a first metablock" ('702 pat., cl. 33); and

F. "programming an updated version of some of the original data [and logical addresses associated with the updated version of the original data] into a second group of one or more pages less than said given number in at least one update block," ('702 pat., cl. 1), "thereafter programming into individual one of a second plurality of pages in a second block, an updated version of less than the given number of pages of the original data programmed into the first plurality of pages" ('702 pat., cl. 16) and "programming the received one or more pages of updated [[user]] data into a second one or more pages of storage block[s]." ('702 pat., cls. 24, 33);

3. In United States Patents Nos. 7,532,511; 7,646,666; and 7,646,667:

A. "defective [block]" ('511 pat., cl. 7);

B. "attach the calculated redundancy codes to the units of user data from

which they are calculated" ('667 pat., cl. 5) and "adding the generated code to the user data from which they are generated" ('511 pat., cl. 1);

C. "generating a redundancy code from the user data of the individual sectors and adding the generated code to the user data from which they are generated" ('511 pat., cl. 1) and "wherein the information of said at least one characteristic of the user data that is stored along with sectors of data includes redundancy codes that have been generated from the user data while the user data is being transferred to the plurality of the first group of blocks, individual ones of the redundancy codes being added to the user data from which they are generated" ('511 pat., cls. 15/14);

D. "storing, in individual ones of the second group of said blocks, information of physical characteristics of the first group of blocks or their operation," ('511 pat., cl. 14), "The method according to claim 1, additionally comprising storing, in one or more of the distinct memory cell blocks other than the plurality of memory cell blocks, data of information related to physical characteristics of the plurality of memory cell blocks or their operation" ('511 pat., cls. 6/1) and "a second group of one or more of the blocks storing records of physical characteristics of the first group of blocks or their operation" ('667 pat., cl. 1);

E. "a record stored in the memory system that contains nonoverlapping ranges of logical addresses of the designated blocks of memory cells within each of the at least two groups, thereby to allow the controller to determine, from a received logical block address, one of the at least two groups in which a corresponding designated block of memory cells is located and the address of the corresponding designated block of memory cells within the determined group" ('666 pat., cl. 1);

F. "a controller adapted to (1) communicate user data between the interface and the first group of blocks with the use of those of the records in the controller memory from the second group of blocks that correspond to those of the first group of blocks with which user data are communicated" ('667 pat., cl. 1); and

G. "a controller adapted to . . . (2) write user data received through the interface into more than one of the blocks of memory cells of the first group

of blocks in more than one sub-array at a time" ('667 pat., cl. 1).

Entered this 27th day of December, 2010.

BY THE COURT:
/s/
BARBARA B. CRABB
District Judge